FDMA1024NZ
Dual N-Channel PowerTrench® MOSFET
20 V, 5.0 A, 54 mΩ

Features
- Max rDS(on) = 54 mΩ at VGS = 4.5 V, ID = 5.0 A
- Max rDS(on) = 66 mΩ at VGS = 2.5 V, ID = 4.2 A
- Max rDS(on) = 82 mΩ at VGS = 1.8 V, ID = 2.3 A
- Max rDS(on) = 114 mΩ at VGS = 1.5 V, ID = 2.0 A
- HBM ESD protection level = 1.6 kV (Note 3)
- Low profile - 0.8 mm maximum - in the new package MicroFET 2x2 mm
- RoHS Compliant
- Free from halogenated compounds and antimony oxides

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Dual N-Channel PowerTrench® MOSFET
20 V, 5.0 A, 54 mΩ

General Description
This device is designed specifically as a single package solution for dual switching requirements in cellular handset and other ultra-portable applications. It features two independent N-Channel MOSFETs with low on-state resistance for minimum conduction losses.

The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Applications
- Baseband Switch
- Loadswitch
- DC-DC Conversion

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
<th>Units</th>
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<tbody>
<tr>
<td>V_DS</td>
<td>Drain to Source Voltage</td>
<td>20</td>
<td>V</td>
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<tr>
<td>V_GS</td>
<td>Gate to Source Voltage</td>
<td>±8</td>
<td>V</td>
</tr>
<tr>
<td>I_D</td>
<td>Drain Current -Continuous</td>
<td>(Note 1a)</td>
<td>5.0 A</td>
</tr>
<tr>
<td></td>
<td>-Pulsed</td>
<td>6.0 A</td>
<td></td>
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<tr>
<td>P_D</td>
<td>Power Dissipation</td>
<td>(Note 1a)</td>
<td>1.4 W</td>
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<tr>
<td></td>
<td>(Note 1b)</td>
<td>0.7 W</td>
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<tr>
<td>T_J, T_STG</td>
<td>Operating and Storage Junction Temperature Range</td>
<td>-55 to +150 °C</td>
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Thermal Characteristics

<table>
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<th>Symbol</th>
<th>Parameter</th>
<th>Ratings</th>
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<tr>
<td>R_{JJA}</td>
<td>Thermal Resistance, Junction to Ambient</td>
<td>(Note 1a)</td>
<td>86 (Single Operation) °C/W</td>
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<tr>
<td>R_{JJA}</td>
<td>Thermal Resistance, Junction to Ambient</td>
<td>(Note 1b)</td>
<td>173 (Single Operation) °C/W</td>
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<td>R_{JJA}</td>
<td>Thermal Resistance, Junction to Ambient</td>
<td>(Note 1c)</td>
<td>69 (Dual Operation) °C/W</td>
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<tr>
<td>R_{JJA}</td>
<td>Thermal Resistance, Junction to Ambient</td>
<td>(Note 1d)</td>
<td>151 (Dual Operation) °C/W</td>
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Package Marking and Ordering Information

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<tr>
<th>Device Marking</th>
<th>Device</th>
<th>Package</th>
<th>Reel Size</th>
<th>Tape Width</th>
<th>Quantity</th>
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<tr>
<td>024</td>
<td>FDMA1024NZ</td>
<td>MicroFET 2X2</td>
<td>7&quot;</td>
<td>8 mm</td>
<td>3000 units</td>
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### Electrical Characteristics \( T_J = 25 \, ^\circ C \) unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<td><strong>Off Characteristics</strong></td>
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<tr>
<td>( BVDSS )</td>
<td>Drain to Source Breakdown Voltage ( I_D = 250 , \mu A, V_{GS} = 0 , V )</td>
<td>20</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>( \Delta BV_{DSS} )</td>
<td>Breakdown Voltage Temperature Coefficient ( I_D = 250 , \mu A, ) referenced to 25 °C</td>
<td>19</td>
<td>mV/°C</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>( IDSS )</td>
<td>Zero Gate Voltage Drain Current ( V_{DS} = 16 , V, V_{GS} = 0 , V )</td>
<td>1</td>
<td>( \mu A )</td>
<td></td>
<td></td>
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<tr>
<td>( IGSS )</td>
<td>Gate to Source Leakage Current ( V_{GS} = \pm 8 , V, V_{DS} = 0 , V )</td>
<td>( \pm 10 ) ( \mu A )</td>
<td></td>
<td></td>
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| **On Characteristics** |                                            |               |     |     |     |       |
| \( V_{GS(th)} \)     | Gate to Source Threshold Voltage \( V_{GS} = V_{DS}, I_D = 250 \, \mu A \) | 0.4           | 0.7 | 1.0 | V   |       |
| \( \Delta V_{GS(th)} \) | Gate to Source Threshold Voltage Temperature Coefficient \( I_D = 250 \, \mu A, \) referenced to 25 °C | -3            | mV/°C |     |     |       |
| \( r_{DS(on)} \)    | Static Drain to Source On-Resistance \( V_{GS} = 4.5 \, V, I_D = 5.0 \, A \) | 37            | 54 |     |     |       |
|                     | \( V_{GS} = 2.5 \, V, I_D = 4.2 \, A \) | 43            | 66 |     |     |       |
|                     | \( V_{GS} = 1.8 \, V, I_D = 2.3 \, A \) | 52            | 82 |     |     |       |
|                     | \( V_{GS} = 1.5 \, V, I_D = 2.0 \, A \) | 67            | 114|     |     |       |
|                     | \( V_{GS} = 4.5 \, V, I_D = 5.0 \, A, T_J = 125 \, ^\circ C \) | 51            | 75 |     |     |       |
| \( g_{FS} \)       | Forward Transconductance \( V_{DD} = 5 \, V, I_D = 5.0 \, A \) | 16            | 75 |     |     |       |

| **Dynamic Characteristics** |                                            |               |     |     |     |       |
| \( C_{iss} \)     | Input Capacitance \( V_{GS} = 10 \, V, V_{GS} = 0 \, V \), \( f = 1 \, MHz \) | 375           | 500 |     |     | pF   |
| \( C_{oss} \)     | Output Capacitance \( V_{DS} = 10 \, V, V_{GS} = 0 \, V \), \( f = 1 \, MHz \) | 70            | 95  |     |     | pF   |
| \( C_{iss} \)     | Reverse Transfer Capacitance \( V_{GS} = 4.5 \, V, V_{DD} = 10 \, V \), \( f = 1 \, MHz \) | 40            | 65  |     |     | pF   |
| \( R_G \)        | Gate Resistance \( f = 1 \, MHz \) | 4.3           |     |     |     | Ω    |

| **Switching Characteristics** |                                            |               |     |     |     |       |
| \( t_{(on)} \)      | Turn-On Delay Time \( V_{DD} = 10 \, V, I_D = 5.0 \, A \) | 5.3           |     | 11  |     | ns   |
| \( t_r \)           | Rise Time \( V_{GS} = 4.5 \, V, R_{GEN} = 6 \, \Omega \) | 2.2           |     | 10  |     | ns   |
| \( t_{(off)} \)     | Turn-Off Delay Time \( V_{GS} = 4.5 \, V, R_{GEN} = 6 \, \Omega \) | 18            |     | 33  |     | ns   |
| \( t_f \)           | Fall Time \( V_{GS} = 4.5 \, V, R_{GEN} = 6 \, \Omega \) | 2.3           |     | 10  |     | ns   |
| \( Q_g \)          | Total Gate Charge \( V_{GS} = 4.5 \, V, V_{DD} = 10 \, V \), \( I_D = 5.0 \, A \) | 5.2           |     | 7.3 |     | nC   |
| \( Q_{gs} \)       | Gate to Source Gate Charge \( V_{GS} = 4.5 \, V, V_{DD} = 10 \, V \), \( I_D = 5.0 \, A \) | 0.6           |     |     |     | nC   |
| \( Q_{gd} \)       | Gate to Drain "Miller" Charge \( I_D = 5.0 \, A \) | 0.9           |     |     |     | nC   |

| **Drain-Source Diode Characteristics** |                                            |               |     |     |     |       |
| \( I_S \)          | Maximum Continuous Source-Drain Diode Forward Current \( V_{GS} = 0 \, V, I_S = 1.1 \, A \) (Note 2) | 1.1           |     |     |     | A    |
| \( V_{SD} \)       | Source to Drain Diode Forward Voltage \( I_D = 5.0 \, A \), \( V_{GS} = 0 \, V \) | 0.7           |     | 1.2 |     | V    |
| \( t_{rr} \)        | Reverse Recovery Time \( I_F = 5.0 \, A, \, di/dt = 100 \, A/\mu s \) | 19            |     | 35  |     | ns   |
| \( Q_{rr} \)       | Reverse Recovery Charge \( I_F = 5.0 \, A, \, di/dt = 100 \, A/\mu s \) | 5             |     | 10  |     | nC   |
Notes:

1. \( R_{\theta JA} \) is determined with the device mounted on a 1 in\(^2\) oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. \( R_{\theta JC} \) is guaranteed by design while \( R_{\theta JA} \) is determined by the user's board design.
   - (a) \( R_{\theta JA} = 86 \, {^\circ}C/W \) when mounted on a 1 in\(^2\) pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For single operation.
   - (b) \( R_{\theta JA} = 173 \, {^\circ}C/W \) when mounted on a minimum pad of 2 oz copper. For single operation.
   - (c) \( R_{\theta JA} = 69 \, {^\circ}C/W \) when mounted on a 1 in\(^2\) pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For dual operation.
   - (d) \( R_{\theta JA} = 151 \, {^\circ}C/W \) when mounted on a minimum pad of 2 oz copper. For dual operation.

2. Pulse Test: Pulse Width < 300 us, Duty Cycle < 2.0 %

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
Typical Characteristics  $T_J = 25 \, ^\circ\text{C}$ unless otherwise noted

Figure 1. On-Region Characteristics

Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

Figure 3. Normalized On-Resistance vs Junction Temperature

Figure 4. On-Resistance vs Gate to Source Voltage

Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs Source Current
Typical Characteristics  $T_J = 25 \, ^\circ C$ unless otherwise noted

**Figure 7.** Gate Charge Characteristics

**Figure 8.** Capacitance vs Drain to Source Voltage

**Figure 9.** Gate Leakage Current vs Gate to Source Voltage

**Figure 10.** Forward Bias Safe Operating Area

**Figure 11.** Single Pulse Maximum Power Dissipation
Figure 12. Junction to Ambient Transient Thermal Response Curve

Typical Characteristics \( T_J = 25 \, ^\circ\text{C} \) unless otherwise noted
Dimensional Outline and Pad Layout

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCC EXCEPT AS NOTED.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

⚠️ NON-JEDEC DUAL DAP

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<td>Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
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